

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicants: Jun MURATA et al.  
Application No.: Not yet assigned  
Filed: February 10, 2004  
For: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE HAVING  
SWITCHING MISFET AND CAPACITOR ELEMENT AND  
METHOD OF PRODUCING THE SAME, INCLUDING WIRING  
THEREFOR AND METHOD OF PRODUCING SUCH WIRING  
Group: Not yet assigned  
Examiner: Not yet assigned

**CLAIM FOR PRIORITY**

Mail Stop Patent Application  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

February 10, 2004

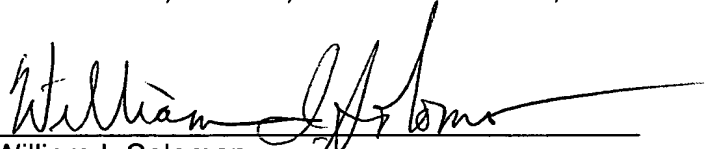
Sir:

Pursuant to the provisions of 35 USC §119 and 37 CFR §1.55, Applicants hereby claim the right of priority based on Japanese Patent Application Nos. 62-235906, 62-235909, 62-235910, 62-235911, 62-235912, 62-235913 and 62-235914, each filed in Japan on September 19, 1987.

Certified copies of each of the above-listed Japanese Patent Applications were filed on September 19, 1988 in Prior Application No. 07/246,514, filed September 19, 1988.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP

  
\_\_\_\_\_  
William I. Solomon  
Registration No. 28,565

WIS/sdb  
(703) 312-6600